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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/559,757	04/27/2000	Yoshio Ozawa	04329.2306	2923

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EXAMINER	
PHAM, THANH V	

ART UNIT	PAPER NUMBER
2823	

DATE MAILED: 06/28/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)
	09/559,757	OZAWA ET AL.
	Examiner	Art Unit
	Thanh V. Pham	2823

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *11 May 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *8-15,20 and 21* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *8-15 and 20-21* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 05/11/2005 has been entered.

Response to Amendment

Claim Rejections - 35 USC § 103

2. The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

3. Claims 8-15 and 20-21 are rejected under 35 U.S.C. 103(a) as being unpatentable over applicants' admitted prior art in combination with Hisamune US Patent No 6,414,352 B1, Aminzadeh et al. US Patent No 6,707,120 B1 and Wolf et al., Silicon Processing for VLSI Era, vol. 1, chapters 6-7.

In the description of the prior art of fig. 15, the applicants disclose that an insulating film 95 containing silicon and nitrogen is formed on the substrate 91; a film 93 which must be processed and which contains silicon is formed on the insulating film; those films are processed such that a portion of the insulating film is exposed to the outside; the structure obtained in the previous steps is subjected to an oxidation

process (the instant specification, page 7, lines 4-5; page 18, lines 21-22; page 20, line 26 to page 21, line 1).

The applicants' admitted prior art does not provide, in the oxidation step, a surface of the semiconductor substrate is lowered, oxidizing gas containing one of ozone and oxygen radicals, the oxygen radicals being generated by remote plasma oxidizing method or by reacting a first gas containing oxygen and a second gas containing hydrogen and *a concentration of nitrogen of the part of the insulating film under an edge portion of the film being decreased by the thermal oxidation process* (the added limitation in the amended claims 8 and 12).

The Hisamune reference discloses oxidation processes are required after forming the gates (col. 2, lines 56-57) and recognizes that, "in the oxidation processes, oxygen radical created within a furnace easily diverges through the separating regions in the form of silicon dioxide and reaches the gates... This encroachment of the oxide into the bottom of the gates is known as a "gate bird's beak" because of its shape when viewed in cross-section" (col. 2, line 64 to col. 3, line 7). The teaching of Hisamune accords with the teaching of Wolf et al. pages 198, 202, 211, 215-221, 227-228 on Thermal Oxidation, chapter 7 *wherein the surface of the semiconductor substrate is lowered (fig. 3, page 202)* and pages 183-187, 191-195 on Chemical Vapor reaction, chapter 6 wherein plasma oxidation and oxygen/hydrogen reacting are taught *(fig. 7, page 171, fig. 6, page 170, fig. 8, page 172, page 184 and fig. 18, page 186, e.g.)*.

The applicant's admitted prior art teaches "bird's beak oxidation owing to the post oxidation" (the instant specification, page 20's last line), the Hisamune reference also

concerns about the gate bird's beak free technology (col. 1, line 9 and col. 3, line 6). To employ the oxidation process with oxidizing gas containing one of ozone and oxygen radicals of Hisamune, supported by Wolf et al., to the oxidation process of applicants' admitted prior art would have been obvious to one of ordinary skill in the art as the oxidizing gas containing one of ozone and oxygen radicals, *the oxygen radicals being generated by remote plasma oxidizing method (Wolf's fig. 6, page 170, fig. 7, page 171, fig. 8, page 172, e.g.) or by reacting a first gas containing oxygen and a second gas containing hydrogen (Wolf's page 184 and fig. 18, page 186, e.g.),* as recognized as conventional by Hisamune would be selected in order *to lower the surface of the semiconductor substrate,* to have a bird-beak free in insulating layer (Hisamune's col. 1, line 9) in accordance with the oxidation step as taught by applicants' admitted prior art.

"Lowering a surface of the semiconductor substrate under a part of the insulating film than a surface of the semiconductor substrate under the film which is processed to cause the portion of the insulating film to be exposed to the outside by applying a thermal oxidation process to a semiconductor structure obtained in the step of an oxidation process by using the oxidizing gas containing one of ozone and oxygen radicals" is inherent as recognized by Aminzadeh et al., figs. 2, 6 and the corresponding passages, (the inherency of "lowering the surface" is supported by Wolf et al.'s fig. 3, page 202.) Further, with the explanation of Wolf's fig. 2, page 201, in according to fig. 3, page 202, the incorporation of oxidant into the Si/SiO_2, in this case, the insulating film containing silicon and nitrogen, would reduce the concentration of nitrogen of the part of the insulating film under an edge portion of the film by the thermal oxidation process.

Re claim 20-21, the Wolf et al. reference, in fig. 4, page 205, teaches a plot at various temperatures between 700 and 1300 ^{O}C as a function of oxidation time.

Choice of temperature within a particular time frame would have been a matter of routine optimization because temperature and time are known to affect device properties and would depend on the desired device density on the finished wafer and the desired device characteristics. One of ordinary skill in the art would have been led to the recited temperature through routine experimentation to achieve desired deposition and reaction rates.

Although Wolf et al. teaches broadly nitridation of silicon dioxide (page 210), the reference does not teach the step of subjecting this particular structure to at least one of a nitriding process and an additional oxidation process. "Improvement in the quality of the film owing to recovery of the process damage becomes insufficient" (applicant's admitted prior art, page 21, lines20-22).

The Aminzadeh et al. reference discloses a process of Kusunoki et al. in IEEE IEDM, vol. 91, wherein the re-oxided nitrided oxide applied on the gate structure could increase the thickness of side oxide 201, fig. 2 and last line of col. 1. With its own invention, the Aminzadeh et al. reference discloses "the poly reox step forms oxide 600 on the gate electrode 403, and also increase the thickness of gate oxide 404 over the areas that will become the source and drain regions", col. 3, last line to col. 4, line 2. The "oxide 600 is then nitridated to strengthen the oxide", "the nitridation can be performed in a furnace or a RTP", col. 4, lines 22 and 34-35. The gate structure is

subjected to the oxidizing process to at least one of nitriding process and an additional oxidation process as in fig. 7 and the related explanation in col. 4, line 42 to col. 6, line 30.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to apply further the nitridation and anneal steps of Aminzadeh et al. into the above combination of Hisamune with applicants' admitted prior art as a further process step would be selected in order to strengthened the gate dielectric film in accordance with the oxidation step as taught by Aminzadeh et al.

The concentration of 5×10^{13} cm^{-2} nitrogen in the interface of silicon oxynitride film with the silicon substrate would have been an obvious matter of design choice bounded by well known manufacturing constraints and ascertainable by routine experimentation and optimization to choose this particular concentration to overcome applicants' admitted prior art constraint (specification's page 21), and it appears that the process would possess utility using this concentration.

Response to Arguments

1. Applicant's arguments filed 05/11/2005 have been fully considered but they are not persuasive.

2. In response to applicant's arguments against the references individually, one cannot show nonobviousness by attacking references individually where the rejections are based on combinations of references. See *In re Keller*, 642 F.2d 413, 208

USPQ 871 (CCPA 1981); *In re Merck & Co.*, 800 F.2d 1091, 231 USPQ 375 (Fed. Cir. 1986).

3. Applicant's argument on pages 8-9 attacks Hisamune's invention while the rejection uses Hisamune's teaching on the required oxidation processes after forming the gates and Hisamune's recognization that, in the oxidation processes, oxygen radical created within a furnace easily diverges through the separating regions in the form of silicon dioxide and reaches the gates. This encroachment of the oxide into the bottom of the gates (known as a "gate bird's beak" because of its shape when viewed in cross-section, col. 2, line 64 to col. 3, line 7) is in combination with applicant's admitted prior art of the structure prior to thermal oxidation. The applicant's admitted prior art has "an insulating film 95 containing silicon and nitrogen" and "a film 93 which must be processed and which contains silicon". This formed structure of applicant's admitted prior art will endure the thermal oxidation of Hisamune to have the semiconductor substrate's surface lowered and the concentration of nitrogen decreased (these symptoms are supported by Wolf).

4. Applicant's argument at the end of page 8 unto page 9 attacks Wolf's CVD "cannot produce a bird's beak" and states that "the process disclosed in Wolf is a CVD process not the thermal oxidation process" and "Wolf still does not establish ... "an insulating film containing silicon and nitrogen"" in page 10. The title of chapter 7 is Thermal Oxidation. The examiner already provides copy of chapter 7 (and chapter 6, because in chapter 6 some helpful definitions could be used to understand chapter 7 and alternatively, chapter 7 refers to chapter 6 on ways of oxidation) that supports

the process of Hisamune on the formed structure of applicant's admitted prior art. Wolf is not used for "an insulating film containing silicon and nitrogen" but the applicant's admitted prior art is. Further, as stated in the first page of chapter 7, "there are several ways to produce SiO_2 directly on the Si surface, it is most often accomplished by thermal oxidation, in which the silicon is exposed to an oxidizing ambient (O_2, H_2O) at elevated temperatures. Thermal oxidation is capable of producing SiO_2 films with controlled thickness and Si/SiO_2 interface properties", "The oxidation of polysilicon is discussed in Chap. 6". With that point of view, thermal oxidation and CVD process are ways of forming SiO_2.

5. In response to applicant's arguments on page 10, these arguments are respectfully traversed because, although not taught as a preferred embodiment, Hisamune teaches this embodiment nonetheless, and disclosed examples and preferred embodiments do not constitute a teaching away from a broader disclosure or nonpreferred embodiments. In re Susi, 169 USPQ 423 (CCPA 1971). "A known or obvious composition does not become patentable simply because it has been described as somewhat inferior to some other product for the same use." In re Gurley, 31 USPQ2d 1130, 1132 (Fed. Cir. 1994). A reference may be relied upon for all that it would have reasonably suggested to one having ordinary skill the art, including nonpreferred embodiments. Merck & Co. v. Biocraft Laboratories, 874 F.2d 804, 10 USPQ2d 1843 (Fed. Cir.), cert. denied, 493 U.S. 975 (1989). Even a teaching away from a claimed invention does not render the invention patentable. See Celeritas Technologies Ltd. v. Rockwell International Corp., 150 F.3d 1354, 1361, 47 USPQ2d

1516, 1522-23 (Fed. Cir. 1998), where the court held that the prior art anticipated the claims even though it taught away from the claimed invention. "The fact that a modem with a single carrier data signal is shown to be less than optimal does not vitiate the fact that it is disclosed." To further clarify, a prior art opinion that a claimed invention is not preferred for a particular limited purpose, does not preclude utility of the invention for that or another purpose, or even preferability of the invention for another purpose. The pointed to passages (Hisamune's col. 1, lines 9-10 and col. 3, lines 24-28) are different from another passage that the examiner directs to (col. 2, line 64 – col. 3, line 7) wherein different position of the structure is mentioned.

6. Applicant's argument in the paragraph bridges page 10 and page 11 on the last limitation of claim 12 is responded as in the above. Further, the re-oxided nitrided oxide applied on the gate structure of applicant's admitted prior art could increase the thickness of side oxide 201 as pointed out by Aminzadeh et al. (fig. 2 and last line of col. 1 about the prior art of Kusunoki et al.) The same performance as of the instant invention that increases the thickness of side oxide would also make the surface of the obtained semiconductor substrate lower.

7. The argument on the newly added limitation in claims 8 and 12 is addressed in the rejection.

8. In response to applicant's argument that the examiner has combined an excessive number of references, reliance on a large number of references in a rejection does not, without more, weigh against the obviousness of the claimed invention. See *In re Gorman*, 933 F.2d 982, 18 USPQ2d 1885 (Fed. Cir. 1991).

Conclusion

9. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

10. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thanh V. Pham whose telephone number is 571-272-1866. The examiner can normally be reached on M-T (6:30-5:00).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Olik Chaudhuri can be reached on 571-272-1855. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

TVP

06/15/2005

George Fourson
Primary Examiner